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MICROMACHINED STIMULATING ELECTRODES

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MICROMACHINED STIMULATING ELECTRODES

Summary

This program seeks to develop a family of two- and three-dimensional active stimulating probes for use in neural prostheses. Two active probes, STIM-1B (monopolar) and STIM-1A (bipolar) have been completed. A four-channel 64-site multipolar probe, STIM-2B is now being completed. This probe allows each of four externally-generated currents to be steered to one of 16 sites under the direction of a digital address delivered to the probe. A three-dimensional version of this probe, STIM-3B, is also nearing completion. Following these probes, the design of a 64-site 8-channel probe, STIM-2, will be iterated, and this probe will also be fabricated, completing this second-generation family of devices.

During the past quarter, the deposition of parylene on these probes was explored. The parylene was removed from the sites using laser ablation. Using a large metal area, the exposed site was defined by how large the ablated area was. (The laser ablated the parylene over only a portion of the total metal area.) The resulting impedances were as expected, with no sign of parylene adhesion problems. During the coming term, we plan to further explore the use of such probes in-vivo and in-vitro. We have also continued to explore the use of a porous silicon layer for probe fabrication. This layer would allow the retention of probes having a lightly-doped bulk area. The circuit areas would thus not be affected by the release etch, which could be done at low temperatures due to the very high surface-to-volume ratio of the porous sacrificial area. An n+ buried layer appears to be an ideal sacrificial layer, and the first probe substrates using this process have been successfully formed. While this process may not replace the boron etch-stop for cortical devices, it could be very useful in active ribbon probes such as those needed for cochlear implantation.

The first run of STIM-2B probes was completed during the past term. Full functionality of the digital circuitry was confirmed through testing; however, the n-channel MOS threshold levels on this run were significantly higher than their design targets, rendering the analog circuitry (the recording amplifiers) inoperable. The problem was traced to the inadvertent removal of the masking photoresist over the nMOS device areas during the field implant, which caused the field implant to penetrate the p-well areas. The results correlate very well with both spreading resistance doping profiles and device simulations. A new run of these probes has begun, and working devices are expected during the next reporting period. The external electronics is ready for use with these probes, and we hope to operate the entire system in in-vivo experiments this spring.

MICROMACHINED STIMULATING ELECTRODES

1. Introduction

The goal of this research is the development of active multichannel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully and distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data which can be demultiplexed on the probe to provide access to a large number of stimulating sites. Our goal in this area is to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes which are then applied to the tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in previous reports, we have designed a series of active probes containing CMOS signal processing electronics. Two of these probes have been completed and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is now undergoing a final iteration and is a second-generation version of our original high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the per-channel current amplitudes. STIM-1A and -1B offer a biphasic range using ±5V supplies from 0μA to ±254μA with a resolution of 2μA, while STIM-2 has a range from 0 to ±127μA with a resolution of 1μA. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-1B is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. It will be the backbone of a multi-probe three-dimensional (3D) 1024-site array (STIM-3) now in development. A new probe, STIM-2B, is currently being added to this set. It offers 64-site capability with off-chip generation of the stimulus currents for four separate channels. These channels are organized in four groups so that each current can be directed to any of the 16 sites in its group, and the site can be programmed for either stimulation or recording. This probe will be available in both 2D and 3D versions (as STIM-2B/3B).

During the past quarter, we have continued to fabricate passive probe structures for internal and external users. We have also continued to explore the use of porous silicon as a sacrificial layer in probe formation as a possible alternative to a boron etch-stop in some situations. The use of parylene ablation has also been explored for site formation. Finally, the first of the STIM-2B/3B probes have been fabricated and tested. The results in each of these areas are described more fully in the sections below.

2. *Use of Parylene Ablation for Post-Processing Site Formation*

In previous quarterly reports, we described the process of coating silicon probes with parylene. Parylene is known for its protective characteristics, its biocompatibility, and for increasing the stiffness of longer probes. We recently asked PI Medical to ablate selective areas of the total site area on a number of probes. It was our hope that we could create a generic-sized site, cover it with parylene and then define the site area to suit the intended use. The study thus addresses the ability of parylene to adhere tightly around an ablated opening and is key to a number of applications of this technology. For this study, PI Medical coated SX04 electrodes with 1μm of parylene. The two sites closest to the tip had an ablated area of 10μm x 10μm, the next two sites had an ablated area of 15μm x 15μm, and the top site had an ablated area of 20μm x 20μm (Fig. 1).

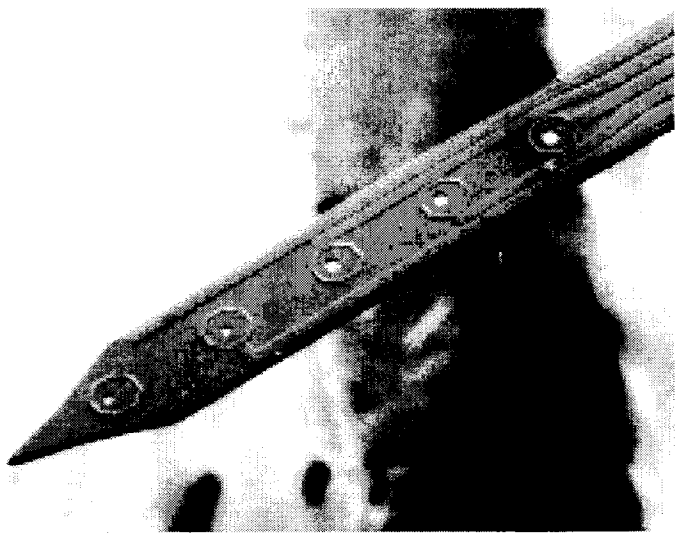

Fig. 1: Scanning Electron Micrograph of an SX04 electrode coated with parylene. Portions of the total site area were ablated to expose areas of 10μm x 10 μm (tip two sites), 15μm x 15μm (next two sites), and 20μm x 20μm (top site).

Figures 2 and 3 show the CV and impedance measurements taken. There was a slight difference for the CV and impedance measurements for the various sized openings. The CV measurements showed that the smallest ablated openings (10μm x 10μm) had the least charge storage capacity; the largest ablated openings (20μm x 20μm) had the greatest charge storage capacity, as should be expected. The impedance measurements showed that the smallest sized opening (10μm x 10μm) had the highest impedance where as the largest sized opening (20μm x 20μm) had the smallest impedance. This also, is what is to be expected. We took the site conductance and divided it by the ablated area to see if conductance was constant per area. Figure 4 shows a plot of this with frequency. At lower frequencies (≤ 1kHz), the partially-ablated sites were nearly identical. At frequencies

above 1 kHz, the smaller-area sites increased at a faster rate than the larger sites. We then normalized the data to the 20μm x 20μm ablated area site. This is shown in Fig. 5. The 15μm x 15μm sites and the 10μm x 10μm sites both lie within the predicted perimeter and area ratios for a site of that size. This is encouraging in that the ablated sites are behaving as a normal site of that size would. We see no signs of parylene lifting around the sites. During the next quarter we will soak these sites and pulse test them in-vitro and use them in-vivo to further assess their performance.

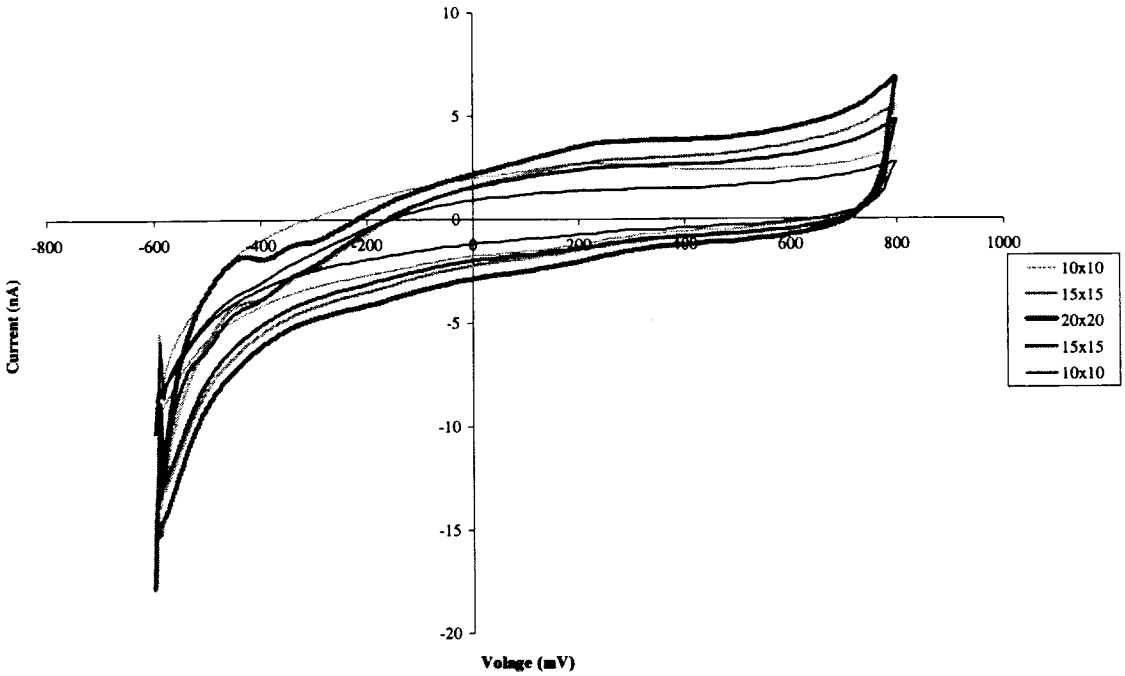

Fig. 2: Cyclic voltammograms of ablated sites for different ablation areas.

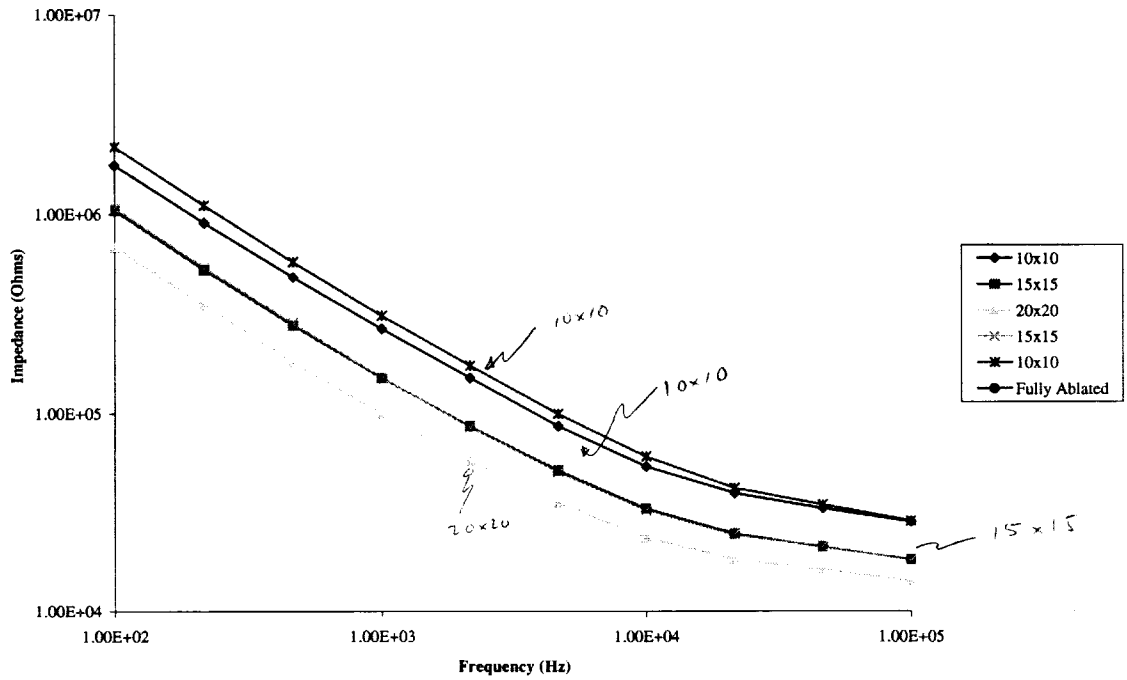

Fig. 3: Site impedance as a function of frequency for different ablation areas.

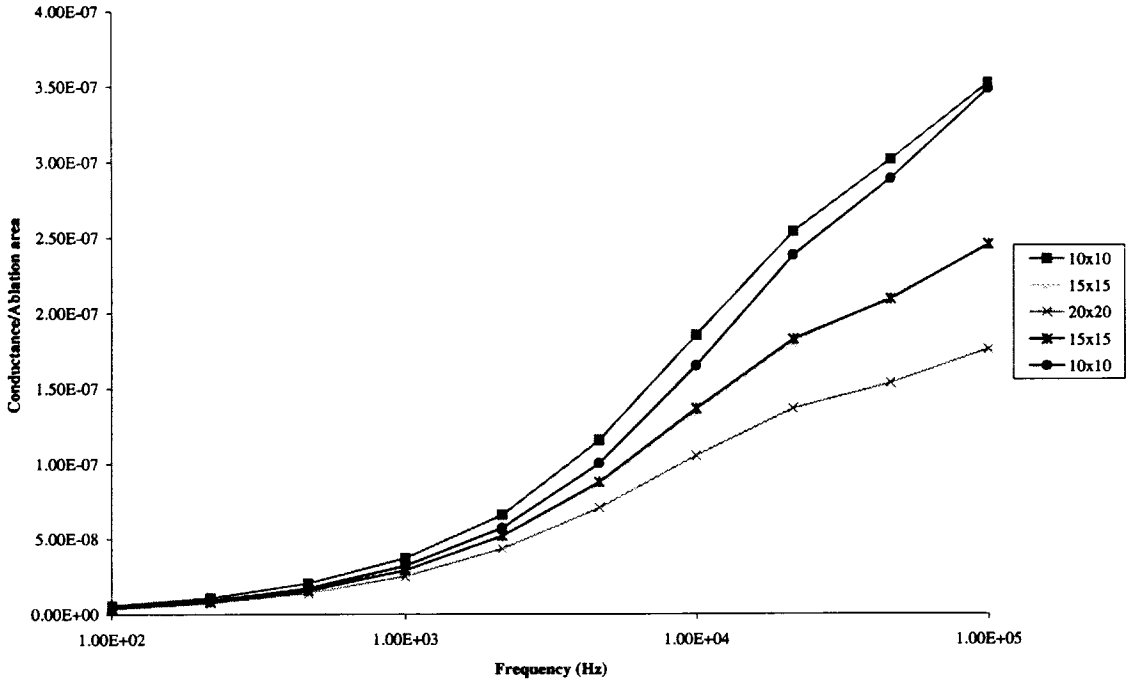

Fig. 4: Conductance per unit area of ablated sites as a function of frequency for different ablated areas.

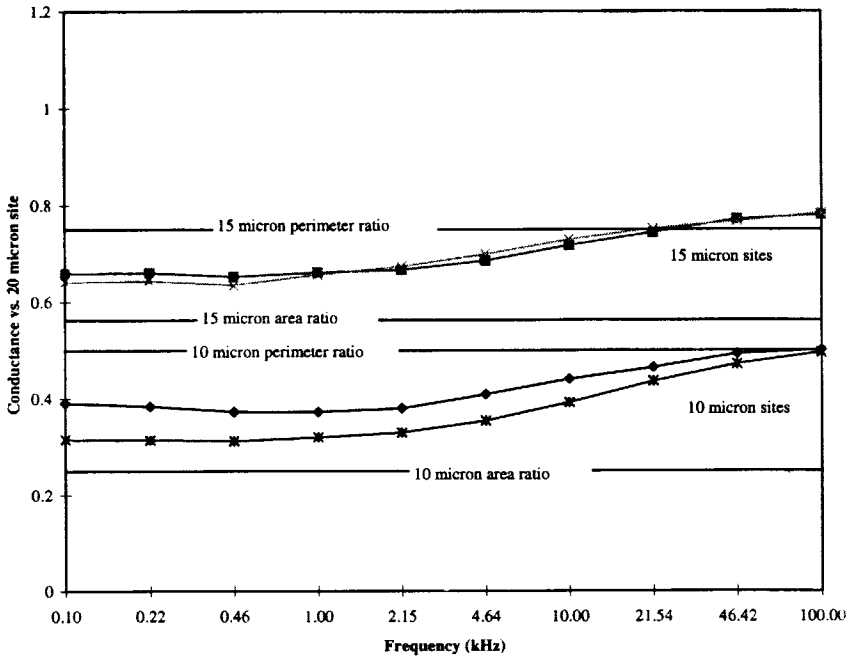

Fig. 5: Site conductance, normallized to a 20μm site, as a function of frequency for different site sizes.

3. *Porous Silicon Micromachining Process Development*

Significant progress has been made on the development of an alternative micromachining process, which uses a porous silicon sacrificial layer. As described in previous reports, the primary advantage of this technique is its ability to produce lightly-doped bulk silicon structures, thereby allowing the fabrication of distributed circuitry on active devices. Since it does not require a heavily-doped boron etch-stop, resulting structures may be lightly-doped while still providing the necessary etch-stop. An additional etch-stop would therefore be provided beneath circuit areas which is lacking in our current process. This process would also allow some circuitry to be moved from the back-end of active probes to the shanks if desired. This is important for cochlear implant devices, which are ribbon cables supporting many stimulating sites over a length of 25mm. Distributing site-selection circuitry along the length of the cable would reduce the length and thus the resistance of the site conductors.

A mask set was designed and used to produce the first probe substrates fabricated using the porous silicon technique. Shown in Fig. 6, these structures were defined using a low-dose implant and an 8-hour drive-in, resulting in a junction depth of 6μm and a surface concentration of approximately $2x10^{16}cm^{-3}$, consistent with MOS device fabrication. Access slots, 10μm x 300μm and spaced 200μm apart, are provided to facilitate complete lateral undercutting of the structures via the porous silicon sacrificial layer. Because of the very high surface-to-volume ratio of the porous material, normal anisotropic silicon etches will remove it rapidly at room temperature, where they do not attack normal silicon or any of the other materials used in the probes.

Additional tests have been performed to continue characterization of the process, especially the formation of the porous silicon layer. Epitaxial silicon may be used to form the probe substrates as an alternative to defining them by implant. If this option is used, a heavily-doped buried layer several microns thick may be placed beneath the epitaxial silicon. It has been found that this significantly increases the rate of pore formation in the lateral direction, while decreasing the thickness of the porous layer. Since pore formation increases with doping levels, pores form almost exclusively in the buried layer rather than in the lightly-doped field. This is very important for several reasons. The increased rate of lateral pore formation decreases the time needed to form the sacrificial layer, and the decreased porous layer thickness improves wafer strength for subsequent wafer processing. Both of these factors allow the distance between access holes to be increased, reducing interference with structures on the probes. An example of sacrificial layer formation using a buried layer is shown in Fig. 7. In this sample, the current density in the buried layer was high enough to cause electropolishing, or etching of the porous layer as it was formed. Decreasing the current density results in a porous layer rather than a gap, which is critical if subsequent processing is to be performed.

Based on the fabrication and tests done this quarter, several changes have been made to the proposed porous silicon micromachining process. It was previously thought that devices would be defined by ion implantation, as was done in the case of the probe substrates fabricated this quarter. However, the use of epitaxial silicon has been found to provide several critical advantages, which we believe to be worth the increase in process complexity. The point in the process flow at which sacrificial layer formation will take place has also been changed. While it was previously thought that the porous silicon would be performed at the beginning of the process, we now believe that it would be more appropriate to perform this step after all high-temperature furnace steps have been completed. This prevents the porous layer from being exposed to high temperatures, which have been found to change the structure of porous silicon, making it more difficult to

remove in a silicon etchant. Secondly, since the back side of the wafer must be metallized to form porous silicon, it is desirable to keep the wafers out of all "clean" furnaces after this step. The new process flow is diagrammed in Fig. 8. During the next quarter, process characterization will continue and a run will be started in which probes containing active site-selection circuitry will be fabricated using this process.

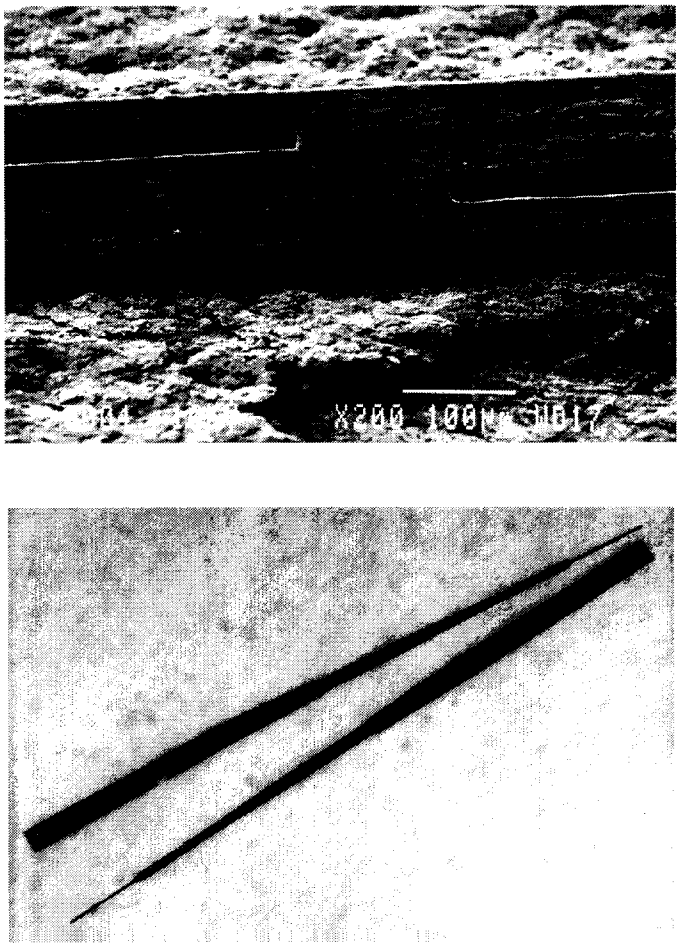

Fig. 6: Lightly-doped p-type neural probe substrates micromachined using an n-type porous silicon sacrificial layer. The structures are 500μm wide at the back end and 14.3mm long. Access holes were provided to facilitate complete lateral undercutting during porous silicon formation.

4. Active Stimulating Probe Development

During the past quarter, work on the development of active stimulating probes has primarily focused on completing the fabrication and testing of the STIM-2B/STIM-3B probe mask set, which is a 16-mask process which includes the deep/shallow boron CMOS process and the three-mask site process. The CMOS circuitry was completed and tested. Testing has demonstrated that the digital portions of the probe circuitry, which is most of the design, all function properly; however, the n-channel MOS threshold was high on this run, preventing the analog circuitry from being operational. Through extensive testing and

analysis, including spreading resistance analysis and simulations, we have identified the processing error which caused the problem. The NMOS active area was not properly protected during the p-field implant. This will be corrected in a new run that has been initiated.

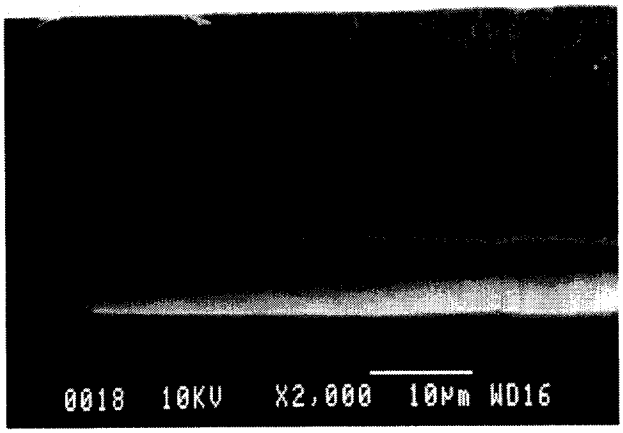

Fig. 7: P-type epitaxial silicon undercut by anodically etching an n+ buried layer. Electropolishing, or removal of a porous silicon layer as it is formed, has taken place here. The n+ layer is etched selectively over the n- field; and the small area of the buried layer results in a high current density, which causes electropolishing. A lower current density results in the buried layer being made porous, which is desirable so that subsequent processing can be performed. The rate of etching in the lateral direction, as seen here, is extremely high compared to that in the vertical etch rate due to the high doping selectivity of pore formation.

STIM-2B

STIM-2B is a second-generation probe, a version of our simplest active stimulating probe, STIM-1B. STIM-2B is a four-channel, 16-shank, 64-site probe which routes four externally generated stimulus signals to 1-of-16 sites per channel. The fabrication of the CMOS circuitry has now been completed and the full functionality of the digital circuitry has been verified through testing. STIM-2B is expected to provide an important tool for performing some key experiments by allowing acute and chronic stimulation in a relatively large volume of neural tissue without mechanically repositioning the probe. This capability is realized by utilizing a 20b shift register to load four 4b site addresses, which are decoded by a 1-of-16 nand-type decoder to connect the desired site to an analog input/output pad through a large CMOS passgate transistor, thereby 'steering' an externally generated current to the addressed site. A newly-added recording function has been added and is activated by a fifth bit (stimulate/record) included with the 4b site address. This fifth bit selects between stimulation and recording by selecting either a direct path to the I/O pad from the site or a path through an amplifier from the same site. Each I/O channel has its own amplifier so that the functionality of all of the channels is independent of each other except for the up-front data input circuitry. The probe was designed to be very robust in that it should function even if the device target parameters were not met exactly. The only portion of the probe that is device parameter sensitive is the amplifier used in the recording mode. The design is such that the probe should still function normally in the stimulation mode if the amplifiers should not work due to device parameter shifts.

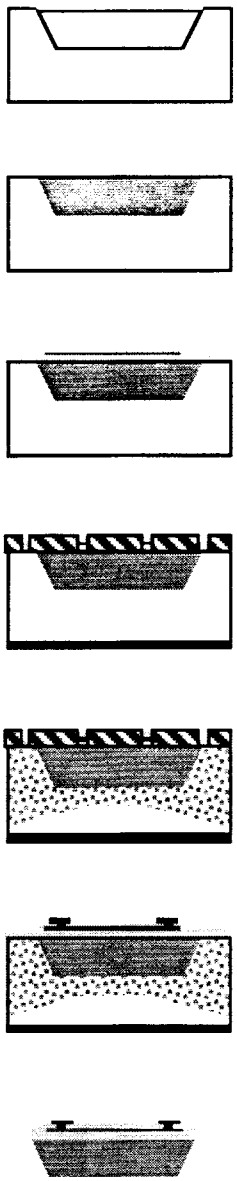

Fig. 8: Process flow for fabricating probes using epitaxial silicon to define the devices and a porous silicon sacrificial layer to release them from the wafer.

A photograph of a completed STIM-2B probe is shown in Fig. 9. Testing of the device parameters revealed that there was a significant problem with one of the device parameters, the NMOS threshold voltage. The NMOS threshold voltage was found to be much higher than design target. The circuit testing and the results will be discussed below. An important result of the testing on this probe was that in spite of the problem with the device threshold voltage, the digital logic could be made to work, thereby demonstrating its proper functionality.

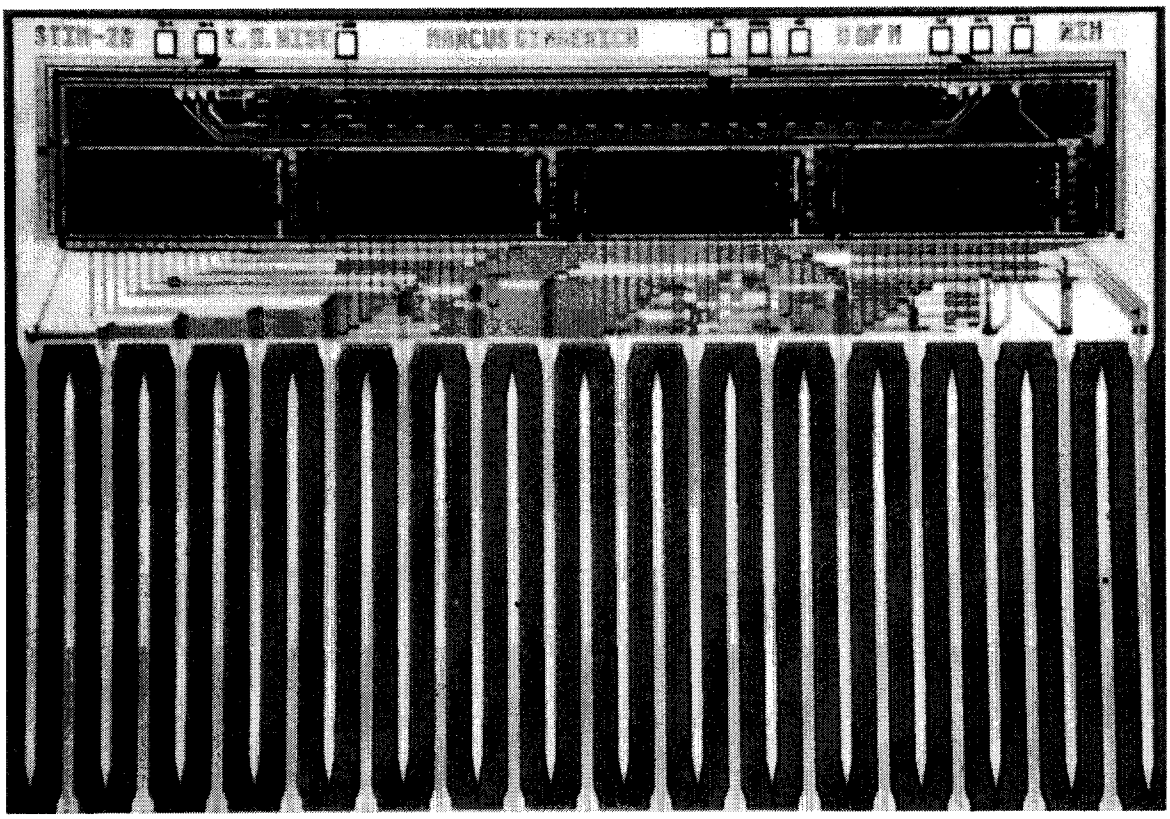

Fig. 9: A photograph of the STIM-2B probe. The shanks are on 400μm centers with four sites per shank.

STIM-3B

STIM-3B is a 3-dimensional probe that is an extension of the 2-D probe, STIM-2B, and is set up to allow use as a device in chronic experiments. There are not any significant differences in these two probe designs, just some structural modifications to allow interconnection to a 3-D platform assembly and a few minor circuit enhancements to allow the addressing of multiple probes in a 3-D array.

The structural changes that are required, some of which can be seen in the photograph of the STIM-3B probe of Fig. 10, include the addition of 'wings' for 3-D stabilization and 'out-riggers' with the integrated beam-lead interconnects for assembly and lead transfer from each probe to the 3D platform assembly. Also seen in the photograph are the 45° slots on the wings, which were designed such that a continuous trench would be etched from the front side of the probe even before the etch plane advances from the backside during the final release etch in EDP. As discussed in previous reports, the integrity of the circuit area was ensured by making the surrounding deep boron diffused rim wide enough so that lateral undercutting from the corners does not have time to reach the active circuit area. The newly developed corner protection technique using dielectric bridges and the anisotropy of the EDP etchant was also used to help improve the yield. Previous etch-out tests demonstrated the effectiveness of this technique.

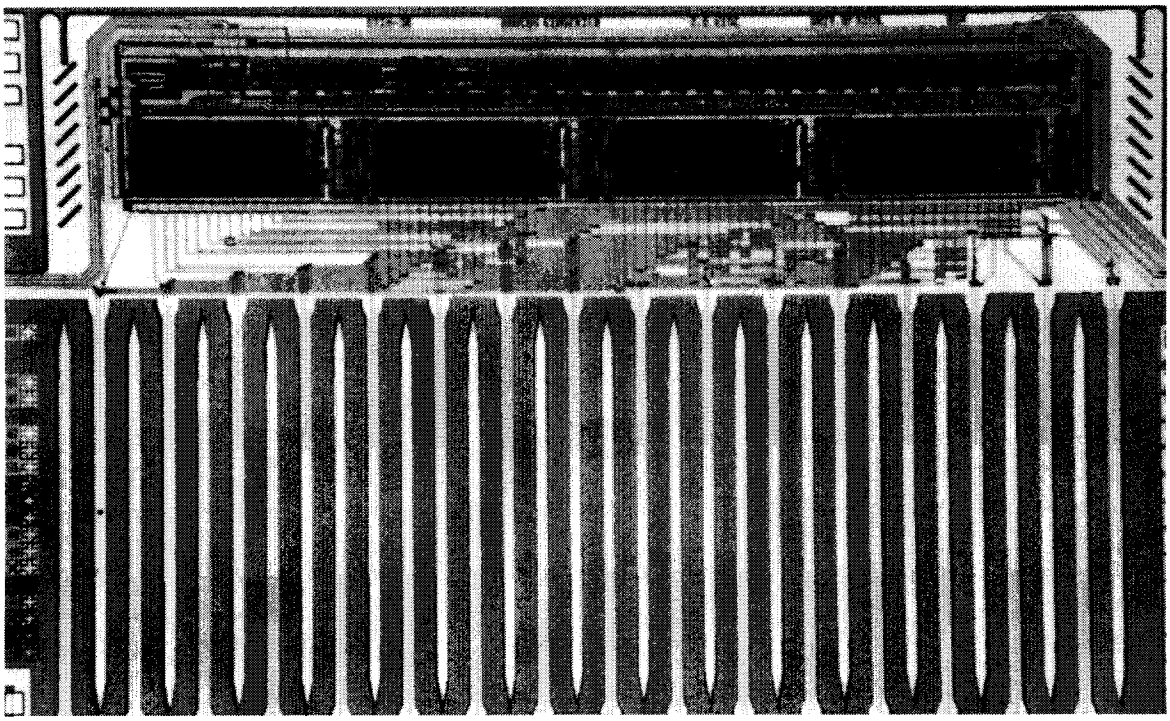

Fig. 10: A photograph of a STIM-3B probe. The shanks are on 400μm centers.

The minimal circuit changes necessary for realization of STIM-3B included adding a 4b shift register which flags the selection of an I/O line via a large CMOS passgate in the line. The last bit of the shift register is then buffered back out. This allows all the probes of a 3D system to share common analog I/O data lines, power lines, clock lines and y-addr (normal probe address) lines. The same y-addr is clocked into all the probes. Simultaneously, an x-addr (channel I/O enable) is clocked into the first probe and then daisy-chained to each successive probe in the array, making an extended 'virtual register.' This allows for different size arrays with only minor changes in addressing from the outside drive circuitry. This allows for a very flexible system with a variable array size, inter-probe stimulation, and almost any combination of four sites across the array. The only weakness is that the same I/O channel cannot be driven on more than one probe simultaneously with an independent stimulus current.

Circuit Testing Results

As mentioned previously, the majority of the testing results confirmed the expected operation from this probe design. Many of the problems that have caused yield problems in the past were overcome. The contact resistances were all very good, with the highest being the contact between the metal interconnect and the p+ source and drain regions, which averaged 1.34Ω/contact with a maximum of 1.49Ω/contact. The PMOS transistor threshold voltage was measured to be -1.06V, which is slightly higher than the expected -0.8V. Though not exactly on target, the PMOS threshold voltage would not cause any significant changes in the overall functionality of the circuitry of these probes. The device parameter that was much further from the target value was the NMOS threshold voltage.

The NMOS threshold voltage was measured to be near 4V instead of the 1V target value. This high NMOS level was not in itself a serious problem for the portion of the circuitry which operates from ±5V rails since the 10V range allows for a swing of over 5V above the threshold voltage. The problem arises in that portion of the circuitry which operates over the standard 0-5V range, i.e., in the shift registers. These circuits do not function very well due to the small fraction voltage swing remaining above threshold over this supply range. This prevents the NMOS transistors from turning on completely. Because of this, the scaled down inverters of the SRAM cells that make up the shift register are not able to properly change states. However, if the ground rail is pulled down to the -5V supply, the extra swing above the NMOS threshold voltage enables the 0-5V logic to function as well. With the circuit powered in this manner, we were able to verify the functionality of the digital logic.

Proper functionality of the probe logic is demonstrated by the scope traces included below. In Figs. 11-14, the bottom trace is the clock signal, the middle trace is the input data and the top trace is a signal as recorded from various points in the probe circuitry. In Fig. 11, the upper trace shows the level-shifted output of bit-19 of the input shift register. The data is appropriately delayed 20 clock cycles and inverted due to the level shifter. The Fig. 12 upper trace correctly shows the signal which controls the large CMOS passgate of channel A, site 0, which as expected is selected (turned on) except when there is at least a single one somewhere in its 4b address. The top trace of Fig. 13 shows the control signal for the CMOS passgate of channel A, site 1, which turns on as soon as the first one is clocked into the first bit of the 4b address of channel A. Finally, the top trace of Fig. 14 shows the control signal for the same site, site 0, of a different channel, channel C. It can be seen that the site is selected on the eleventh clock cycle after the first one of the input data word is shifted through the 10 bits of the previous two channel addresses, channels A and B. These are a few examples demonstrating that the digital input and decoding portions of the probe work as designed. The analog portion of the probe, the amplifiers and strobe detectors, could not be tested, but those circuit blocks are essentially the same as those used in previous probes and their functionality has therefore been demonstrated previously.

An obvious need is to identify the cause of the high nMOS threshold. In this regard, a processing error, if identified, is much more welcome than an equipment problem since the latter can be corrected and is an indicator that if processed correctly we will get what we seek. The latter would indicate random equipment difficulties that would be more difficult to deal with. Fortunately, the former is the case. We got exactly what we should have gotten, given the process that was run. Since only the nMOS threshold was affected and since this threshold is primarily dependent on the surface doping concentration of the p-well, then is would seem likely that surface concentration of the p-well was too high. There are two reasons that could explain a high surface concentration: either the p-well ion implant dose was too large, or the post-implant thermal budget during the remainder of the fabrication process was not as high as expected, resulting in the surface concentration not relaxing as much as expected.

In an attempt to resolve the cause of the problem, a spreading resistance analysis was done by Solecon Labs, Inc., to measure the p-well doping profile under the NMOS gate. A spreading resistance analysis allows the doping concentration to be measured and plotted versus depth into the surface of the wafer. It was expected that if it was simply a case of the implant dose being too high, the doping concentration profile would reveal a high surface concentration with a fairly normal junction depth. On the other hand, if the thermal budget was too low, the doping profile would have a higher than normal surface concentration, but a shallower than normal junction depth. The resulting doping profile is shown in Fig. 15. The profile shows the three expected doping regions, with the p-type

well nearest the surface, the n-type epitaxial layer underneath, and finally the p-type substrate. The unexpected feature was the very high tail of p-type doping concentration near the surface of the p-well. This is obviously <u>not</u> part of a normal profile resulting from the p-well implant and subsequent thermal relaxation. It was also too high to be a result of the threshold adjust implant for the NMOS devices.

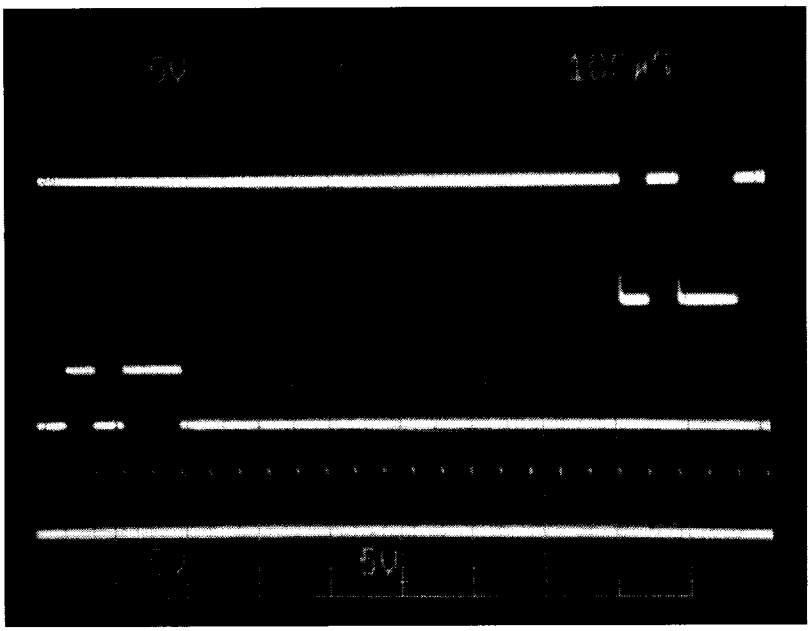

Fig. 11: A scope trace showing (top to bottom): the level shifted output of bit-19 of the input shift register; input data; and clock.

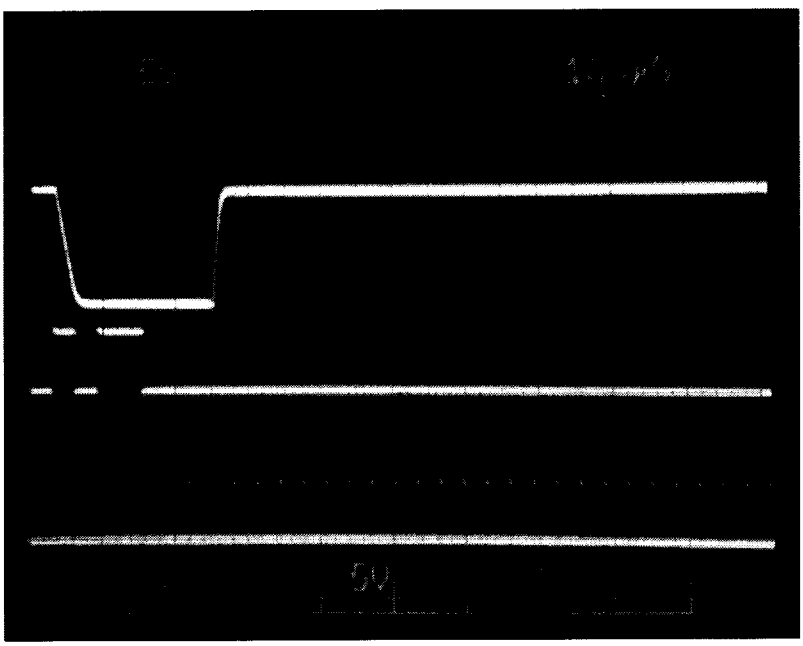

Fig. 12: A scope trace showing (top to bottom): the control signal for channel A, site 0; input data; and clock.

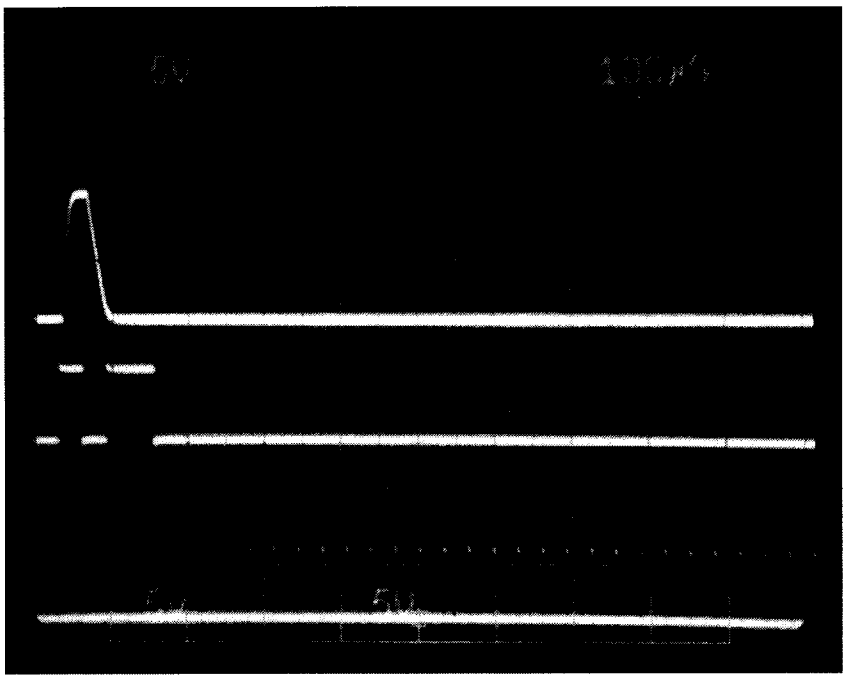

Fig. 13: A scope trace showing (top to bottom): the control signal for channel A, site 1; input data; and clock.

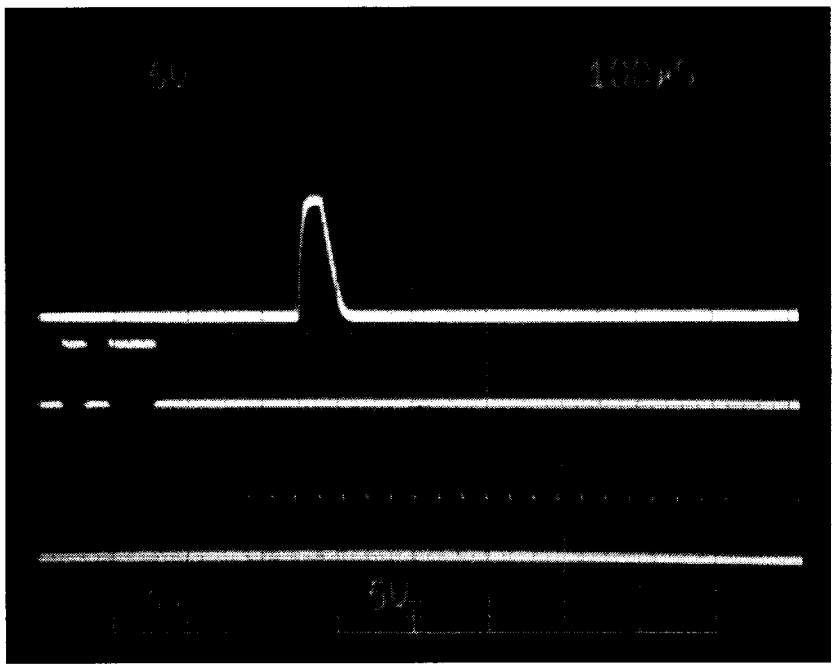

Fig. 14: A scope trace showing (top to bottom): the control signal for channel C, site 1; input data; and clock.

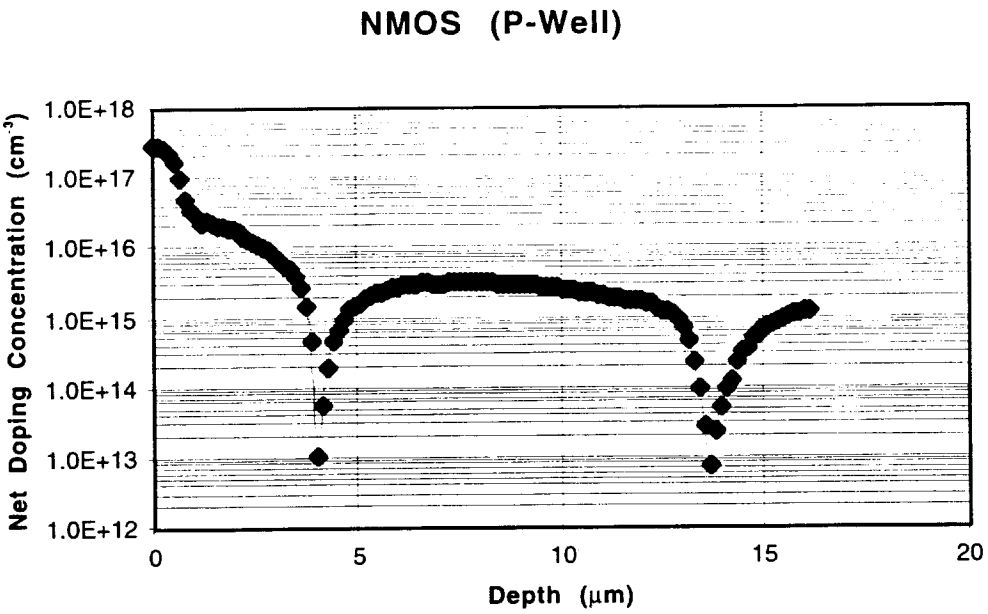

Fig. 15: The doping profile as measured by a spreading resistance analysis, which reveals the doping regions from the surface (left to right): p-type well, the n-type epitaxial layer and finally the p-type substrate. The abnormal peak within the first micron of the surface elevates the doping level there an order of magnitude, taking the NMOS threshold with it.

Using the fabrication process simulator, SUPREM, a complete simulation was performed to mimic the fabrication process as it was actually done from lab notes and process flow sheets. The resulting doping profile is shown in Fig. 16 which is a very close match to the measured profile. By looking at the various steps, the cause of the highly doped surface peak in the p-well was found to be due to improper masking of the NMOS active area during the p-field implant. In the CMOS process flow, after the active area nitride has been etched and just before the field oxide (FOX) is grown, the field area is implanted in order to increase the field threshold voltage so that no parasitic transistors are turned on during normal circuit operation. The p-field implant is a boron implant at an energy of 80keV, which is high enough that some of the implant will actually penetrate all the way through the nitride and pad oxide that still remains over the active areas. (The implant range for boron at 80keV is about 0.35μm, well more than the combined pad oxide and nitride layer thicknesses). The photoresist remaining on the active area after etching the nitride is thick enough to provide the necessary protection against the field implant if it is left in place (as it must be). Unfortunately, on this run it was inadvertantly stripped before the field implant. A simulation of the case in which a thin layer of photoresist, 0.5μm, was left on the active area produced the profile shown in Fig.17, which results in an NMOS threshold of 0.8V, which is the process target. Thus, the high thresholds were due to incorrectly stripping the masking oxide from the active areas prior to the field implant, allowing the implant to penetrate the nitride/oxide dielectrics and dope the active areas excessively. The PMOS active areas were unaffected because the p-field masking step only exposes the p-well active areas and not the portions of the active areas where PMOS transistors are to be formed.

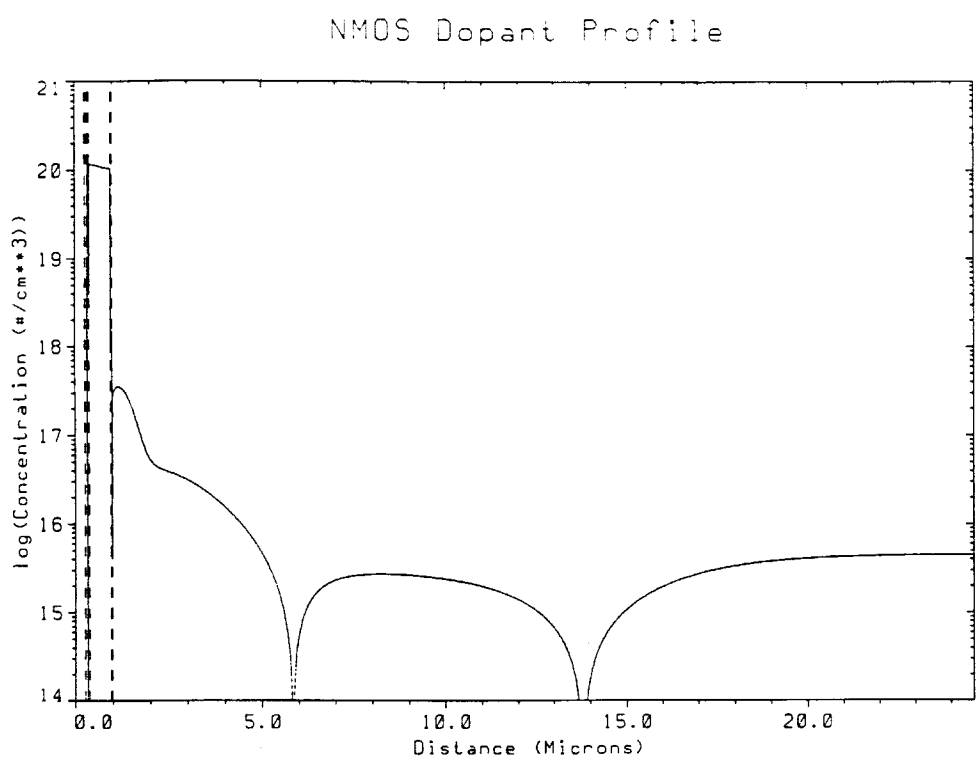

Fig. 16: The simulated NMOS doping profile if no extra protection in addition to the pad oxide and LOCOS nitride were in place over the NMOS active areas during the p-field implant.

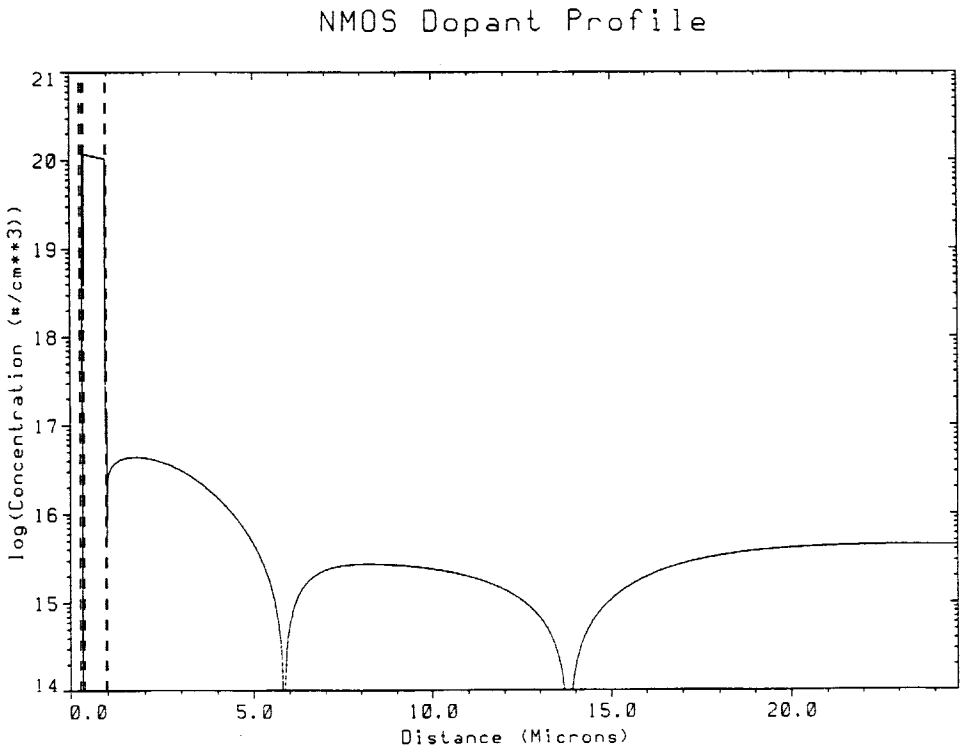

Fig. 17: The simulated NMOS doping profile when an extra layer of photoresist protection is in place over the NMOS active areas during the p-field implant.

There is a slight risk of the same thing occurring in the case of the PMOS transistors during the n-field implant, but because the implant is done with phosphorus and at a lower energy, the amount of dopant that actually penetrates to the silicon surface in the active areas is almost negligible. (The range for phosphorus at 60keV is only about 0.08μm in silicon, considerably less than the pad oxide and nitride, even with no photoresist present). The simulations did reveal a slight shift in the PMOS threshold with an extra layer of photoresist over the active area compared with the same implant without it. This could explain the slightly higher than normal PMOS threshold voltage.

While it is unfortunate that the results of the just-completed CMOS run were not all that was hoped for, a number of benefits have come from the run. Testing demonstrated that the logic of the current design functions as expected. Also, problems occuring in past processing runs such as high contact resistance appear to be well under control. One very encouraging piece of anecdotal information that was noted during the testing was that there was a very high percentage of probes that were functional within the limits of the current device parameters. Almost every probe tested appeared to be functional. A new fabrication run of probes has begun and with the experience gained from the previous run, we anticipate being able to complete the run in as little eight weeks.

In summary, the current run of STIM-2B/3B CMOS wafers was tested and found to function as expected with the exception of a high NMOS transistor threshold voltage. The testing of the probes was able to verify the correct functionality of the logic and demonstrated that for the most part the process looked quite good. The cause of the elevated NMOS transistor threshold voltage was traced to a failure to properly protect the NMOS active areas during the p-field implant, which resulted in part of the p-field implant dose reaching the surface of the p-well. A new fabrication run has begun and is expected to yield fully functional 2-D and 3-D probes during the coming reporting period.

5. External Stimulating Interface System Development

In previous reports we have described the design and construction of an external interface system for active stimulating probes. At the end of the previous quarter this system had been constructed and tested on a wire-wrap carrier. Supporting software was written that enabled basic system testing and operation, as well as simple, manually-driven stimulating tasks.

Work during the past quarter has been directed towards improving the functionality of the host-side software. The goal was to construct a higher-level interface to the remote system, including simple one-step commands for generating pulse waveforms. This goal was achieved by embedding a command-line interpreter, based upon the popular Python interpreted language, into the host-side software. To support this integration, additional software was written to manage the serial communications port (the interface to the remote system). Once the interpreter was embedded in the host-side software, a high-level interface module was written (in the Python language). This module provides a variety of services, such as textual interpretation of various system states, simple state manipulation, and most importantly, a simple command to generate pulsatile waveforms on the remote system. The nature of the embedded interpreter enables rapid prototyping of additional modules or "on-the-fly" implementation of commands in support of testing and stimulation tasks.

During the next quarter we plan to further simplify and improve the host-side software by constructing a graphical user interface (GUI) to the remote system, layered

above the existing embedded interpreter. We expect that this GUI will provide an even higher-level interface to the remote system, thus making it more accessible to users uncomfortable with command-line interfaces. We hope to test this external system with the STIM-2B probes during the coming term.

6. *Conclusions*

This program seeks to develop a family of two- and three-dimensional active stimulating probes for use in neural prostheses. Two active probes, STIM-1B (monopolar) and STIM-1A (bipolar) have been completed. A four-channel 64-site multipolar probe, STIM-2B is now being completed. This probe allows each of four externally-generated currents to be steered to one of 16 sites under the direction of a digital address delivered to the probe. A three-dimensional version of this probe, STIM-3B, is also nearing completion. Following these probes, the design of a 64-site 8-channel probe, STIM-2, will be iterated, and this probe will also be fabricated, completing this second-generation family of devices.

During the past quarter, the deposition of parylene on these probes was explored. The parylene was removed from the sites using laser ablation. Using a large metal area, the exposed site was defined by how large the ablated areas were. (The laser ablated only a portion of the metal area.) The resulting impedances were as expected, with no sign of parylene adhesion problems. During the coming term, we plan to further explore the use of such probes in-vivo and in-vitro. We have also continued to explore the use of a porous silicon layer for probe fabrication. This layer would allow the retention of probes having a lightly-doped bulk area. The circuit areas would thus not be affected by the release etch, which could be done at low temperatures due to the very high surface-to-volume ratio of the porous sacrificial area. An n+ buried layer appears to be an ideal sacrificial layer, and the first probe substrates using this process have been successfully formed. While this process may not replace the boron etch-stop for cortical devices, it could be very useful in active ribbon probes such as those needed for cochlear implantation.

The first run of STIM-2B probes was completed during the past term. Full functionality of the digital circuitry was confirmed through testing; however, the n-channel MOS threshold levels on this run were significantly higher than their design targets, rendering the analog circuitry (the recording amplifiers) inoperable. The problem was traced to the inadvertent removal of the masking photoresist over the nMOS device areas during the field implant, which caused the field implant to penetrate the p-well areas. The results correlate very well with both spreading resistance doping profiles and device simulations. A new run of these probes has begun, and working devices are expected during the next reporting period. The external electronics is ready for use with these probes, and we hope to operate the entire system in in-vivo experiments this spring.